APPEAL BRIEF

IN SUPPORT OF APPELLANT'S APPEAL

TO THE BOARD OF PATENT APPEALS AND INTERFERENCES

Sir:

Applicants (hereafter "Appellants") hereby submit this Brief in triplicate in support of their Appeal from a final decision by the Examiner in the above-captioned case. Appellants respectfully request consideration of this Appeal by the Board of Patent Appeals and Interferences for allowance of the claims in the above-captioned patent application.

An oral hearing is not desired.

I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE UNITED STATES POSTAL SERVICE AS FIRST CLASS MAIL IN AN ENVELOPE ADDRESSED TO:
MAIL STOP APPEAL BRIEF – PATENTS, COMMISSIONER FOR PATENTS, P.O. BOX 1450, ALEXANDRIA, VA 22313-1450, ON: AUGUST 12, 2004.
Date of Deposit

INTEL CORPORATION
Name of Assignee

Anne Collette 8/12/2004
SIGNATURE DATE

08/17/2004 JADD01 00000027 022666 10028860
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I. REAL PARTY IN INTEREST

The invention is assigned to Intel Corporation of 2200 Mission College Boulevard, Santa Clara, California 95052.

II. RELATED APPEALS AND INTERFERENCES

To the best of Appellant's knowledge, there are no appeals or interferences related to the present appeal that will directly affect, be directly affected by, or have a bearing on the Board's decision.

III. STATUS OF THE CLAIMS

Claims 1-20 and 22-29 are currently pending in the above-referenced patent application.

In the Final Office Action mailed May 19, 2004, Claims 10 and 11 were allowed and Claims 1-9, 12-20, and 22-29 were finally rejected. Claims 1-9, 12-20, and 22-29 are the subject of this appeal.

Claims 1-3, 6-9, 12-20, 22-24, and 26-29 stand rejected under 35 U.S.C. §102(b) as being unpatentable over Fujisaki et al. (U.S. patent 5,763,950) (hereafter "Fujisaki").

Claims 4, 22, 23, and 25 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Fujisaki in view of Patel (U.S. patent no. 5,396,403) (hereafter "Patel").

Claim 5 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Fujisaki in view of Patel and further in view of Lin et al. (U.S. patent no. 6,188,578) (hereafter "Lin").

IV. STATUS OF AMENDMENTS

No amendments have been filed subsequent to the Final Rejection.

A copy of all claims on appeal, namely claims 1-9, 12-20, and 22-29, is attached hereto as Appendix A.

V. SUMMARY OF THE INVENTION

A method and apparatus for cooling an integrated circuit die. An integrated circuit package comprises a package substrate, an integrated circuit die having an active surface, and a cooling fluid. In one embodiment, an interposer is disposed between the package substrate and the integrated circuit die. The interposer establishes electrical connectivity between the integrated circuit die and the package

substrate. In one embodiment, the cooling fluid is in contact with the active surface of the integrated circuit die. An active surface may be electrical components are formed on one side of the integrated circuit die. The integrated circuit die, active surface, and/or the interposer may have a surface having microchannels that allows the cooling fluid to make better contact with the integrated circuit die and interposer, respectively.

VI. ISSUES PRESENTED

A. Whether Claims 1-3, 6-9, 12-20, 22-24, and 26-29 are unpatentable under 35 U.S.C. §102(b) over Fujisaki

B. Whether Claims 4, 22, 23, and 25 are unpatentable under 35 U.S.C. §103(a) over Fujisaki in view of Patel.

C. Whether Claim 5 is unpatentable under 35 U.S.C. §103(a) over Fujisaki in view of Patel and further in view of Lin.

VII. GROUPING OF CLAIMS

For the purposes of this appeal:

Claims 1-7 stand or fall together as Group I;

Claims 8 and 9 stand or fall together as Group II;

Claims 12-16 stand or fall together as Group III;

Claims 17-20 and 22-26 stand or fall together as Group IV; and

Claims 27-29 stand or fall together as Group V.

Reasons for separate patentability of the above indicated Claim Groups I-V are presented in the argument section pursuant to 37 C.F.R. §1.192(c)(7).

VIII. ARGUMENT

A. REJECTION OF CLAIMS 1-3, 6-7 (GROUP I), 8 AND 9 (GROUP II), 12-16 (GROUP III), 17-20, 22-24 AND 26 (GROUP IV), AND 27-29 (GROUP V) UNDER 35 U.S.C. §102(b) IS IMPROPER.

The Examiner rejected Claims 1-3, 6-9, 12-20, 22-24, and 26-29 under 35 U.S.C. §102(b) as being unpatentable over Fujisaki. At page 2 of the Final Office action mailed May 19, 2004, the Examiner stated:

> Fujisaki et al ... disclose a integrated circuit chips/package comprising an integrated circuit die having an active surface 11 and a cooling fluid / coolant 235 directly contact and move across the active surface 11, substrate 12, solder bums 13, heat sink 23, interposer, internal pump/fan 133, and external pump 197 for flowing cooling fluid in the circuit. See Fig. 1, 20, 28, and 37.

At pages 4-5 of the Final Office action mailed May 19, 2004, the Examiner stated:

> [W]hen a fluid enters a closed container from one side and leaves or exits form the other side, the fluid spreads in all possible direction in side the container .... Consequently fluid touches all the objects and exchanges heat therewith inside the container before leaving the container from the other end.
>
> Therefore, Fig. 37 constructionally teaches the claimed subject matter. Moreover, Fujisaki describes for Fig. 37 and 38, "Before passing inside the sealed container 231 and reaching an outlet 236, a coolant 235 hits the partition members 220 and forms the two-dimensional jet flow on the downstream side of each partition member 220. Hence, the semiconductor elements 11 are efficiently cooled. In other words, this first modification can utilize the high cooling efficiency of the jet flow and also increase to the limit the mounting density of the semiconductor elements 11 within the electronic equipment."

Claim Group I

In the Final Office Action, mailed on May 19, 2004, the Examiner rejected claims 1-3 and 6-7 under 35 U.S.C. §102(b) as being unpatentable over Fujisaki.

As is well-established, to make a prima facie rejection under 35 USC §102(b), the Examiner must provide a single prior art reference that discloses, expressly or under the principles of inherency, each and every element of a claimed invention. See RCA Corp. v. Applied Digital Data Systems. Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984); Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987); and MPEP section 2131. The

Examiner has failed to make a prima facie rejection of Claims 1-3 and 6-7 under 35 USC §102(b) over Fujisaki.

Claim 1 recites:

An integrated circuit package comprising:

an integrated circuit die having an active surface; and

a cooling fluid to directly contact and move laterally across the active surface.

Claim 1 recites in pertinent part "cooling fluid to directly contact and move laterally across the active surface" (emphasis added). For example, Applicants' specification at page 1, lines 18-20 states:

"electrical components are formed on one side of the integrated circuit die, herein referred to as the "active surface" of the integrated circuit die."

Fujisaki does not teach each and every element of the cited portion of Claim 1. With respect to FIG. 1, Fujisaki discloses "semiconductor element 11" having "top surface 11a" mounted to a "circuit substrate 12 via a plurality of connecting members 13 such as solder" (col. 1, lines 33-36). Fujisaki further discloses "semiconductor element 11 is cooled when a coolant (cooling medium) 15 flows parallel to the circuit substrate 12 and passes the periphery of the semiconductor element 11. In other words, the cooling takes place due to heat exchange between the coolant 15 and the pin-shaped fins 14 and the top surface 11a of the semiconductor element 11" (col. 1, lines 39-44) (emphasis added).

With respect to Fig. 20, Fujisaki discloses at col. 11, lines 33-53:

The fan 35 and the compact fan 133 are driven. When the fan 35 is driven, the air is drawn in as the coolant via the coolant inlet 36, and the parallel coolant flow 43 which is parallel to the circuit substrate 12 is formed within the passage 33. On the other hand, when the compact fan 133 is driven, a parallel coolant flow portion 43-1 which is close to the passage forming member 32 out of the parallel coolant flow 43 is drawn in by the compact fan 133 and is ejected in the form of an ejected coolant flow portion 135 as indicated by an arrow. This ejected coolant flow portion 135 forms an angle .alpha. towards the downstream side of the parallel coolant flow 43 with respect to a line 138 which is perpendicular to the circuit substrate 12.

On the other hand, out of the parallel coolant flow 43, a parallel coolant flow portion 43-2 which is close to the circuit substrate 12 hits the heat sink 131. In addition, the above ejected coolant flow portion 135 also hits the heat sink 131. Hence, the heat of the heat sink 131 is absorbed by both the parallel coolant flow portion 43-2 and the ejected coolant flow portion 135, and the semiconductor element 11 is efficiently cooled. (Emphasis added).

With respect to Fig. 28, Fujisaki discloses at col. 14, lines 1-18:

FIG. 28 shows the third embodiment. In a semiconductor element cooling apparatus 190 shown in FIG. 28, a duct forms the means for obliquely hitting the coolant.

In FIG. 28, the semiconductor element 11 is mounted on the circuit substrate 12, and the heat sink 131 is provided on this semiconductor element 11. A duct 191 has an outlet 192 which is arranged obliquely to the semiconductor element 11. A compact fan 194 is mounted at an inlet 193 of this duct 191.

The parallel coolant flow 43 and an ejected coolant flow 195 which is ejected obliquely from the outlet 192 of the duct 191 hit the semiconductor element 11. Hence, the semiconductor element 11 is efficiently cooled for reasons similar to the case where the compact fan 133 is obliquely arranged as described above. (Emphasis added).

With respect to Figs. 37 and 38, Fujisaki discloses at col. 16, lines 30-50:

In FIGS. 37 and 38, a plurality of circuit substrates 12-1, 12-2 and 12-3 are accommodated within a sealed container 231. The circuit boards 12-1, 12-2 and 12-3 are coupled to a mother board 234 via a connector 233 as shown in FIG. 38. A plurality of semiconductor elements 11 are mounted on each of the circuit substrates 12-1, 12-2 and 12-3 in a matrix arrangement. Each partition member 220 is mounted on the adjacent circuit substrate so as to confront the semiconductor elements 11 on the circuit substrates 12-1, 12-2 and 12-3. With respect to the uppermost circuit substrate 12-1, the partition member 220 is mounted on the inner wall of the sealed container 231.

Before passing inside the sealed container 231 and reaching an outlet 236, a coolant 235 hits the partition members 220 and forms the two-dimensional jet flow on the downstream side of each partition member 220. Hence, the semiconductor elements 11 are efficiently cooled. In other words, this first modification can utilize the high cooling efficiency of the jet flow and also increase to the limit the mounting density of the semiconductor elements 11 within the electronic equipment. (Emphasis added).

Fujisaki does not disclose "cooling fluid to directly contact and move laterally across the active surface" (emphasis added) of Claim 1. Accordingly, the Examiner has not met his burden of a prima facie showing of anticipation of Claim 1 under 35 U.S.C. §102(b) in view of Fujisaki. Accordingly, the rejection of Claim 1 under 35 U.S.C. §102(b) in view of Fujisaki is improper and Claim 1 overcomes the rejection under 35 U.S.C. §102(b) in view of Fujisaki. Claims 2-3 and 6-7 depend from Claim 1 and are allowable over the teachings of Fujisaki for at least the same reason as pertains to Claim 1.

Claim Group II

In the Final Office Action, mailed on May 19, 2004, the Examiner rejected claims 8 and 9 under 35 U.S.C. §102(b) as being unpatentable over Fujisaki.

As is well-established, to make a prima facie rejection under 35 USC §102(b), the Examiner must provide a single prior art reference that discloses, expressly or under the principles of inherency, each and every element of a claimed invention. See RCA Corp. v. Applied Digital Data Systems. Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984); Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987); and MPEP section 2131. The Examiner has failed to make a prima facie rejection of Claims 8 and 9 under 35 USC 102(b) over Fujisaki.

Claim 8 recites:

> A method of forming an integrated circuit package comprising:
>
> attaching an interposer to a package substrate;
>
> attaching an integrated circuit die to the interposer, wherein the integrated circuit die includes an active region;
>
> covering the package substrate, the integrated circuit die, and the interposer with a heat spreader to form an internal chamber;
>
> filling the internal chamber with a cooling fluid, wherein the cooling fluid contacts a region between the interposer and the integrated circuit die and wherein the cooling fluid is to directly contact and move laterally across the active region.

Claim 8 recites in pertinent part "cooling fluid is to directly contact and move laterally across the active region" (emphasis added). For example, Applicants' specification at page 1, lines 18-20 states:

> "electrical components are formed on one side of the integrated circuit die, herein referred to as the "active surface" of the integrated circuit die."

Fujisaki does not teach each and every element of the cited portion of Claim 8. As can be seen from the discussion earlier with respect to Claim Group I, Fujisaki does not teach the cited portion of Claim 8. Accordingly, the Examiner has not met his burden of a prima facie showing of anticipation of Claim 8 under 35 U.S.C. §102(b) in view of Fujisaki. Accordingly, the rejection of Claim 8 under 35 U.S.C.

§102(b) in view of Fujisaki is improper and Claim 8 overcomes the rejection under 35 U.S.C. §102(b) in view of Fujisaki. Claim 9 depends from Claim 8 and is allowable over the teachings of Fujisaki for at least the same reason as pertains to Claim 8.

Claim Group III

In the Final Office Action, mailed on May 19, 2004, the Examiner rejected claims 12-16 under 35 U.S.C. §102(b) as being unpatentable over Fujisaki.

As is well-established, to make a prima facie rejection under 35 USC §102(b), the Examiner must provide a single prior art reference that discloses, expressly or under the principles of inherency, each and every element of a claimed invention. See RCA Corp. v. Applied Digital Data Systems. Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984); Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987); and MPEP section 2131. The Examiner has failed to make a prima facie rejection of Claims 12-16 under 35 USC 102(b) over Fujisaki.

Claim 12 recites:

> A method of cooling an integrated circuit die within an integrated circuit package comprising:
>
> providing power to the integrated circuit die; and
> moving a cooling fluid laterally across and in direct contact with an active surface of the integrated circuit die.

Claim 12 recites in pertinent part "moving a cooling fluid laterally across and in direct contact with an active surface of the integrated circuit die" (emphasis added). For example, Applicants' specification at page 1, lines 18-20 states:

> "electrical components are formed on one side of the integrated circuit die, herein referred to as the "active surface" of the integrated circuit die."

Fujisaki does not teach each and every element of the cited portion of Claim 12. As can be seen from the discussion earlier with respect to Claim Group I, Fujisaki does not teach the cited portion of Claim 12. Accordingly, the Examiner has not met his burden of a prima facie showing of anticipation of Claim 12 under 35 U.S.C. §102(b) in view of Fujisaki. Accordingly, the rejection of Claim 12 under 35 U.S.C.

§102(b) is improper and Claim 12 overcomes the rejection under 35 U.S.C. §102(b) in view of Fujisaki. Claims 13-16 depend from Claim 12 and are allowable over the teachings of Fujisaki for at least the same reason as pertains to Claim 12.

Claim Group IV

In the Final Office Action, mailed on May 19, 2004, the Examiner rejected claims 17-20, 22-24, and 26 under 35 U.S.C. §102(b) as being unpatentable over Fujisaki.

As is well-established, to make a prima facie rejection under 35 USC §102(b), the Examiner must provide a single prior art reference that discloses, expressly or under the principles of inherency, each and every element of a claimed invention. See RCA Corp. v. Applied Digital Data Systems. Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984); Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987); and MPEP section 2131. The Examiner has failed to make a prima facie rejection of Claim 17-20, 22-24, and 26 under 35 USC §102(b) over Fujisaki.

Claim 17 recites:

An integrated circuit package comprising:

a package substrate;

a first integrated circuit die having an active surface;

an interposer disposed between the package substrate and the first integrated circuit die, the interposer establishing electrical connectivity between the first integrated circuit die and the package substrate; and

a cooling fluid disposed between the first integrated circuit die and the interposer, wherein the cooling fluid is to directly contact and move laterally across the active surface.

Claim 17 recites in pertinent part "cooling fluid is to directly contact and move laterally across the active surface" (emphasis added). For example, Applicants' specification at page 1, lines 18-20 states:

"electrical components are formed on one side of the integrated circuit die, herein referred to as the "active surface" of the integrated circuit die."

Fujisaki does not teach each and every element of the cited portion of Claim 17. As can be seen from the discussion earlier with respect to Claim Group I, Fujisaki does not teach the cited portion of Claim 17. Accordingly, the Examiner has not met his burden of a prima facie showing of anticipation of Claim 17 under 35 U.S.C. §102(b) in view of Fujisaki. Accordingly, the rejection of Claim 17 under 35 U.S.C. §102(b) in view of Fujisaki is improper and Claim 17 overcomes the rejection under 35 U.S.C. §102(b) in view of Fujisaki. Claims 18-20, 22-24, and 26 depend from Claim 17 and are allowable over the teachings of Fujisaki for at least the same reason as pertains to Claim 17.

Claim Group V

In the Final Office Action, mailed on May 19, 2004, the Examiner rejected claims 27-29 under 35 U.S.C. §102(b) as being unpatentable over Fujisaki.

As is well-established, to make a prima facie rejection under 35 USC §102(b), the Examiner must provide a single prior art reference that discloses, expressly or under the principles of inherency, each and every element of a claimed invention. See RCA Corp. v. Applied Digital Data Systems. Inc., 730 F.2d 1440, 1444, 221 USPQ 385, 388 (Fed. Cir. 1984); Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987); and MPEP section 2131. The Examiner has failed to make a prima facie rejection of Claims 27-29 under 35 USC §102(b) over Fujisaki.

Claim 27 recites:

An integrated circuit package comprising:

a integrated circuit die housed within a chamber, wherein the integrated circuit die includes an active region; and

a cooling fluid filling the chamber and to directly contact and move laterally across the active region of the integrated circuit die.

Claim 27 recites in pertinent part "a cooling fluid ... directly contact and move laterally across the active region of the integrated circuit die" (emphasis added). For example, Applicants' specification at page 1, lines 18-20 states:

"electrical components are formed on one side of the integrated circuit die, herein referred to as the "active surface" of the integrated circuit die."

Fujisaki does not teach each and every element of the cited portion of Claim 27. As can be seen from the discussion earlier with respect to Claim Group I, Fujisaki does not teach the cited portion of Claim 27. Accordingly, the Examiner has not met his burden of a prima facie showing of anticipation of Claim 27 under 35 U.S.C. §102(b) in view of Fujisaki. Accordingly, the rejection of Claim 27 under 35 U.S.C. §102(b) in view of Fujisaki is improper and Claim 27 overcomes the rejection under 35 U.S.C. §102(b) in view of Fujisaki. Claims 28-29 depend from Claim 27 and are allowable over the teachings of Fujisaki for at least the same reason as pertains to Claim 27.

B. REJECTION OF CLAIM 4 (GROUP I) AND CLAIMS 22, 23, AND 25 (GROUP IV) UNDER 35 U.S.C. § 103(A) AS BEING UNPATENTABLE OVER FUJISAKI IN VIEW OF PATEL IS IMPROPER

The Examiner rejected Claims 4, 22, 23, and 25 under 35 U.S.C. 103(a) as being unpatentable over Fujisaki in view of Patel. At pages 2-3 of the Final Office action mailed May 19, 2004, the Examiner stated:

> Fujisaki et al. do not disclose a coupling feature to the both side of an interposer by solder bums. Patel teaches the use of a coupling feature to the both sides of an interposer 65 by solder bumps 17 in an integrated circuit for purpose of making a desired integrated circuit. Patel also disclose an electrical cable 89 for power connection... Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the integrated circuit chips of Fujisaki et al. in view of Patel such that an a coupling feature of the interposer and solder bumps could be provided in order to make the integrated circuit in a desired manner.

Claim Group I

In the Final Office Action, mailed on May 19, 2004, the Examiner rejected claim 4 under 35 U.S.C. §103(a) as being unpatentable over Fujisaki in view of Patel, now being addressed in this Appeal under separate claim groups.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not

in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) and MPEP 2143. The Examiner has failed to make a prima facie rejection of Claim 4 under 35 USC §103(a) over Fujisaki in view of Patel.

Claim 4 depends from Claim 1. Claim 1 recites:

An integrated circuit package comprising:

an integrated circuit die having an active surface; and

a cooling fluid to directly contact and move laterally across the active surface.

Claim 1 recites in pertinent part "cooling fluid to directly contact and move laterally across the active surface" (emphasis added). For example, Applicants' specification at page 1, lines 18-20 states:

"electrical components are formed on one side of the integrated circuit die, herein referred to as the "active surface" of the integrated circuit die."

As provided in Section A above with respect to Claim Group I, Fujisaki does not teach each and every element of the cited portion of Claim 1. Patel teaches "a plurality of integrated circuit chips 13 mounted on a first surface 15 of the substrate by means of solder bumps 17" (col. 4, lines 46-48). Patel further recites "FIG. 4 illustrates ... substrate 61 that has one or more chips 63 on an upper surface 65 and more chips 67 on a lower surface 69" (col. 6, lines 5-8). Patel fails to teach or suggest the deficiencies of Fujisaki stated with respect to Claim 1 in Section A above with respect to Claim Group I. Fujisaki in view of Patel do not disclose "cooling fluid to directly contact and move laterally across the active surface" (emphasis added) of Claim 1. Claim 4 depends from Claim 1. Accordingly, the Examiner has not met his burden of a prima facie showing of obviousness of Claim 4 under 35 U.S.C. §103(a) over Fujisaki in view of Patel. Accordingly, the rejection of Claim 4 under 35 U.S.C. §103(a) is improper and Claim 4 overcomes the rejection under 35 U.S.C. §103(a) over Fujisaki in view of Patel.

Claim Group IV

In the Final Office Action, mailed on May 19, 2004, the Examiner rejected claims 22, 23, and 25 under 35 U.S.C. §103(a) as being unpatentable over Fujisaki in view of Patel, now being addressed in this Appeal under separate claim groups.

To establish a prima facie case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally

available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) and MPEP 2143. The Examiner has failed to make a prima facie rejection of Claims 22, 23, and 25 under 35 USC §103(a) over Fujisaki in view of Patel.

Claims 22, 23, and 25 depend from Claim 17. Claim 17 recites:

An integrated circuit package comprising:

a package substrate;

a first integrated circuit die having an active surface;

an interposer disposed between the package substrate and the first integrated circuit die, the interposer establishing electrical connectivity between the first integrated circuit die and the package substrate; and

a cooling fluid disposed between the first integrated circuit die and the interposer, wherein the cooling fluid is to directly contact and move laterally across the active surface.

Claim 17 recites in pertinent part "cooling fluid is to directly contact and move laterally across the active surface" (emphasis added). For example, Applicants' specification at page 1, lines 18-20 states:

"electrical components are formed on one side of the integrated circuit die, herein referred to as the "active surface" of the integrated circuit die."

As can be seen in Section B above with respect to Claim Group I, Fujisaki in view of Patel do not disclose "cooling fluid is to directly contact and move laterally across the active surface" (emphasis added) of Claim 17. Claims 22, 23, and 25 depend from Claim 17. Accordingly, the Examiner has not met his burden of a prima facie showing of obviousness of Claims 22, 23, and 25 under 35 U.S.C. §103(a) over Fujisaki in view of Patel. Accordingly, the rejection of Claims 22, 23, and 25 under 35 U.S.C. §103(a) over Fujisaki in view of Patel is improper and Claims 22, 23, and 25 overcome the rejection under 35 U.S.C. §103(a) over Fujisaki in view of Patel.

C. REJECTION OF CLAIM 5 (GROUP I) UNDER 35 U.S.C. § 103(A) AS BEING UNPATENTABLE OVER FUJISAKI IN VIEW OF PATEL AND FURTHER IN VIEW OF LIN IS IMPROPER

Claim Group I

In the Final Office Action, mailed on May 19, 2004, the Examiner rejected claim 5 under 35 U.S.C. §103(a) as being unpatentable over Fujisaki in view of Patel and further in view of Lin, now being addressed in this Appeal under separate claim groups.

As is well-established, to make a prima facie rejection of obviousness under 35 USC 103, the Examiner must provide a prior art document which shows, teaches, suggests, or describes each and every element of the rejected claims. In re Fine, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988); In re Rouffet, 47 USPQ2d 1453, 1457-58 (Fed. Cir. 1998); MPEP 2143.01. The Examiner must also demonstrate a motivation in the prior art to make the asserted combination. In re Linter, 173 USPQ 560, 562 (CCPA 1972); MPEP 2143.01. The Examiner has failed to make a prima facie rejection of Claim 5 under 35 USC §103(a) over Fujisaki in view of Patel and further in view of Lin.

Claim 5 depends from Claim 1. Claim 1 recites:

> An integrated circuit package comprising:
>
> an integrated circuit die having an active surface; and
>
> a cooling fluid to directly contact and move laterally across the active surface.

Claim 1 recites in pertinent part "cooling fluid to directly contact and move laterally across the active surface" (emphasis added). For example, Applicants' specification at page 1, lines 18-20 states:

> "electrical components are formed on one side of the integrated circuit die, herein referred to as the "active surface" of the integrated circuit die."

As can be seen in Section B above with respect to Claim Group I, Fujisaki in view of Patel do not disclose "cooling fluid to directly contact and move laterally across the active surface" (emphasis added) of Claim 1. Lin teaches "an integrated circuit package having a heat spreader to dissipate heat generated by a die both from the backside of the die and by conducting to the printed circuit board, so as to improve the heat dissipating effect" (col. 2, lines 27-33). Lin fails to teach or suggest the deficiencies of Fujisaki in view of Patel stated with respect to Claim 1. Claim 5 depends from Claim 1. Accordingly,

the Examiner has not met his burden of a prima facie showing of obviousness of Claim 5 under 35 U.S.C. §103(a) over Fujisaki in view of Patel and further in view of Lin. Accordingly, the rejection of Claim 5 under 35 U.S.C. §103(a) over Fujisaki in view of Patel and further in view of Lin is improper and Claim 5 overcomes the rejection under 35 U.S.C. §103(a) over Fujisaki in view of Patel and further in view of Lin.

IX. CONCLUSION

Appellants respectfully submit that all the pending claims in this patent application are patentable and request that the Board of Patent Appeals and Interferences overrule the Examiner and direct allowance of the rejected claims and allowed claims 10 and 11.

This brief is submitted in triplicate, along with authorization to charge $320.00 to Deposit Account No. 02-2666 to cover the appeal fee for one other than a small entity as specified in 37 C.F.R. § 1.17(c). Please charge any shortages and credit any overcharges to Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: August 12, 2004

John Patrick Ward
Reg. No. 40,216

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025-1030
(408) 720-8300

X. APPENDIX A: CLAIMS ON APPEAL

1. (Previously Presented) An integrated circuit package comprising:

an integrated circuit die having an active surface; and

a cooling fluid to directly contact and move laterally across the active surface.

2. (Original) The integrated circuit package of claim 1 further comprising:

an interposer coupled to the integrated circuit die.

3. (Original) The integrated circuit package of claim 2, wherein the interposer has a microchannel surface that allows the cooling fluid to flow between the interposer and the active surface of the integrated circuit die.

4. (Original) The integrated circuit package of claim 2 further comprising:

a package substrate, wherein a first side of the interposer is coupled to the package substrate via solder bumps, and a second side of the interposer is coupled to the integrated circuit die via solder bumps.

5. (Original) The integrated circuit package of claim 4 further comprising:

an underfill material disposed substantially between the interposer and the package substrate.

6. (Original) The integrated circuit package of claim 1, wherein the integrated circuit die has a microchannel surface.

7. (Original) The integrated circuit package of claim 1 further comprising:

a pump to circulate the cooling fluid.

8. (Previously Presented) A method of forming an integrated circuit package comprising:

attaching an interposer to a package substrate;

attaching an integrated circuit die to the interposer, wherein the integrated circuit die includes an active region;

covering the package substrate, the integrated circuit die, and the interposer with a heat spreader to form an internal chamber;

filling the internal chamber with a cooling fluid, wherein the cooling fluid contacts a region between the interposer and the integrated circuit die and wherein the cooling fluid is to directly contact and move laterally across the active region.

9. (Original) The method of claim 8, wherein the filling of the internal chamber is done by pumping cooling fluid through a via in the package substrate.

Claims 10 and 11 stand allowed and are not under appeal.

12. (Previously Presented) A method of cooling an integrated circuit die within an integrated circuit package comprising:

providing power to the integrated circuit die; and

moving a cooling fluid laterally across and in direct contact with an active surface of the integrated circuit die.

13. (Original) The method of claim 12, wherein the moving of the cooling fluid is performed by thermal convection.

14. (Original) The method of claim 12, wherein the moving of the cooling fluid is performed by a pump located inside of the integrated circuit package.

15. (Original) The method of claim 12, wherein the moving of the cooling fluid is performed by a pump located outside of the integrated circuit package.

16. (Original) The method of claim 12, wherein the cooling fluid changes phase by evaporating at a first location of the integrated circuit package and condensing at a second location of the integrated circuit package.

17. (Previously Presented) An integrated circuit package comprising:

a package substrate;

a first integrated circuit die having an active surface;

an interposer disposed between the package substrate and the first integrated circuit die, the interposer establishing electrical connectivity between the first integrated circuit die and the package substrate; and

a cooling fluid disposed between the first integrated circuit die and the interposer, wherein the cooling fluid is to directly contact and move laterally across the active surface.

18. (Original) The integrated circuit package of claim 17 further comprising:

a heat spreader covering the package substrate, the first integrated circuit die, the cooling fluid, and the interposer.

19. (Original) The integrated circuit package of claim 18 further comprising:

a heat sink coupled to the heat spreader.

20. (Original) The integrated circuit package of claim 18, wherein the first integrated circuit die has a microchannel surface in contact with the heat spreader, the microchannel surface allowing cooling fluid to flow across the microchannel surface.

21. (Cancelled)

22. (Original) The integrated circuit package of claim 17, wherein the interposer provides electrical functionality in addition to electrical connectivity.

23. (Original) The integrated circuit package of claim 22, wherein the interposer provides capacitance.

24. (Original) The integrated circuit package of claim 22, wherein the interposer comprises a second integrated circuit die.

25. (Original) The integrated circuit package of claim 24, wherein the second integrated circuit provides an optical to electrical interface for the first integrated circuit die.

26. (Original) The integrated circuit package of claim 17, wherein the interposer has a microchannel surface in contact with the active surface of the first integrated circuit die.

27. (Previously Presented) An integrated circuit package comprising:

a integrated circuit die housed within a chamber, wherein the integrated circuit die includes an active region; and

a cooling fluid filling the chamber and to directly contact and move laterally across the active region of the integrated circuit die.

28. (Original) The integrated circuit package of claim 27 further comprising:

a plurality of microchannels in a surface of the integrated circuit die.

29. (Original) The integrated circuit package of claim 28 further comprising:

a pump located within the integrated circuit package to pump the cooling fluid through at least a portion of the plurality of microchannels.